ADGS1412 Data Sheet changes

This document highlights the changes on the data sheet of the ADGS1412 Analog Switch.

Below shows the datasheet section with the removed phrase crossed out and highlighted in red font.

PAGE 1
FEATURES

SPI interface with error detection
Includes CRC, invalid read/write address, and SCLK
    count error detection
Supports burst and daisy-chain mode
Industry-standard SPI Mode 0 ~~and Mode 3~~ Interface-
    compatible
1.5 Ω typical on resistance at 25°C
0.3 Ω typical on-resistance flatness at 25°C
0.1 Ω typical on-resistance match between channels
    at 25°C
Fully specified at ±15 V, ±5 V, and +12 V
V$_{SS}$ to V$_{DD}$ analog signal range

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THEORY OF OPERATION

The ADGS1412 is a set of serially controlled, quad SPST switches with error detection features. SPI Mode 0 ~~and Mode 3~~ can be used with the device, and it operates with SCLK frequencies up to 50 MHz. The default mode for the ADGS1412 is address mode in which the registers of the device are accessed by a 16-bit SPI command that is bounded by CS. The SPI command becomes 24 bit if the user enables CRC error detection. Other error detection features include SCLK count error and invalid read/write error. If any of these SPI interface errors occur, they are detectable by reading the error flags register. The ADGS1412 can also operate in two other modes, namely burst mode and daisy-chain mode.